## REMARKS

Reconsideration and allowance are requested.

Regarding the claim objections, claims 2 and 8 are amended to remove the final closing parenthesis and to enclose the equation in brackets. Claim 7 is amended as suggested by the Examiner. Withdrawal of the objection to the claims is requested.

Claims 2, 4, 6, 8, 10, and 12 stand rejected under 35 U.S.C. §101 for alleged inoperativeness and lack of utility. Given the brackets added to claims 2 and 8, it is clear that the value stored within the three further registers is a new value $Rd_i$ given by the term in the square brackets and not the value of $Rd_i$ currently stored. The new value of $Rd_i$ is given by the exclusive OR of the value of $Rd_i$ currently stored and the inverse of ($X_i$ XOR $Y_i$). Withdrawal of this rejection is requested.

Claims 2, 4, 6, 8, 10, and 12 stand rejected under 35 U.S.C. §112, first paragraph for inadequate written description. The Examiner correctly assumed that claims 5 and 11 contain a typo. They are amended so that the formula is as recited in claims 2 or 8 and Figure 11. Withdrawal of this rejection is requested.

Claims 4-6 and 10-12 stand rejected under 35 U.S.C. §112, second paragraph for inadequate antecedent basis. Claim 4 now depends upon claim 3; claim 5 now depends on claim 4; claim 10 now depends upon claim 9; and claim 11 now depends upon claim 10. This resolves the antecedent basis issues. Withdrawal of this rejection is requested.

In addition, the word "relative" is deleted in claims 1 and 7 to clarify that the number of bits which transition from high to low and from low to high is fixed irrespective of what data value is being written or what data value was previously stored. Example support for this amendment may be found on page 1, last line to page 2, line 2 of the description.

Claims 1, 2, 7, and 9 stand rejected under 35 U.S.C. §103 for obviousness based on Pomet. This rejection is respectfully traversed.

Regarding the claim feature "a register writing circuit operable to store a data value to said data processing register," the Examiner points to the master-slave type flip-flop circuits described at column 1, lines 58-62. From this text, it is not clear what corresponds to the register writing circuit. At column 2, lines 30-33, Pomet discloses a master-slave flip-flop circuit and an "integrated circuit including at least one secured flip-flop circuit. Such [an] integrated circuit is especially suited for registers that are required to process confidential or secret data elements." Thus, Pomet discloses only a circuit which may be used as a data processing register—not a register writing circuit that stores a data value to a data processing register.

Pomet also does not disclose "said register write circuit writes data values to said data processing register such that a fixed number of bits within said data processing register and said three or more further registers as a whole transition from high to low and from low to high irrespective of what data value is being written to said data processing register and what data value was previously stored within said data processing register." Pomet does not ensure that the number of bits which change from high to low and which change from low to high is fixed. In the system of Pomet, "there will always be a switching of two of the loops of the secured D type master-slave flip-flop circuit according to the invention" (column 6, lines 9-11). Thus, Pomet just ensures that the number of loops (or bits) switching is fixed, not that the number of bits switching from high to low and the number of bits switching from low to high are fixed, as recited in claim 1.

This distinction is made clear in Figure 3 of Pomet which shows that the number of bits changing from low to high and from high to low is not constant. Just considering the first few

clock cycles, at the rising edge of the first clock pulse, two loops change from low to high. At the trailing edge of the first clock pulse, those two loops change from high to low. At the rising edge of the second clock pulse, three loops change from low to high, and at the trailing edge of the second clock pulse, one loop NM changes from low to high and loop NSd changes from high to low. Thus, it is clear that the number of high-low and low-high transitions is not fixed.

The office action improperly characterizes the feature as simply that when data is written to multiple flip-flops, "the number of switching events that occurs is always constant." Apparently, the Examiner is using the term "switching event" to simply mean that a 0 or a 1 is written into the flip-flop regardless of the value previously stored. But claims 1 and 8 recite that the fixed number of bits in the register transition from high to low and from low to high irrespective of what data value is being written to the register and what data value was previously stored in the register. Thus Pomet does not disclose or render obvious this feature of claims 1 and 8.

Applicants appreciate the indication of allowable subject matter in claims 2, 4-6, 8, and 10-12. Applicants agree that the combination of features recited in each of the independent claims is patentable. To the extent that the Examiner's reasons for allowance are inconsistent with or add addition limitations to the claims, Applicants respectfully disagree because the claims define the invention.

The application is in condition for allowance. An early notice to that effect is earnestly solicited.

Respectfully submitted,

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